What is claimed is:

1. A frame memory device comprising:

a number of memory cells aligned in a matrix form;

a range selectable column address decoder for receiving first and second column addresses and generating at least one successive column address selection signal in order to designate at least one successive column address range with respect to the number of memory cells; and

a range selectable row address decoder for receiving first and second row addresses and generating at least one successive row address selection signal in order to designate at least one successive row address range with respect to the number of memory cells,

wherein a graphic data write operation is accomplished all at a time with respect to the number of memory cells selected by the at least one successive column address selection signal and the at least one successive row address selection signal.

2. The frame memory device of claim 1, wherein if the first and second column addresses equal each other and the first and second row addresses do not equal each other, a number of memory cells are selected on a single straight line parallel with the Y-axis corresponding to the successive addresses between the first and second row addresses, and if the first and second row addresses equal each other and the first and second column addresses do not equal each other, a number of memory cells are selected on a single straight line parallel with the X-axis corresponding to the successive addresses between the first and second column addresses.

3. The frame memory device of claim 1, wherein if the first and second column addresses do not equal each other and the first and second row addresses do not equal each other, all memory cells are selected in a rectangle corresponding to the successive addresses between the first and second column addresses and the successive addresses between the first and second

row addresses.

4. The memory device of claim 1, wherein the range selectable column address decoder and the range selectable row address decoder perform selection of an address of a successive range, respectively, in which the total 256 addresses are divided into 16 groups in the case that the first and second column addresses and the first and second row addresses are 8-bit signals, respectively, a corresponding group by respective four upper bits of the first and second address inputs in units of 16 addresses, a low address range is selected among 16 addresses in the group selected by four lower bits of the low address input among the first and second addresses, a high address range is selected among 16 addresses in the group selected by four lower bits of the high address input among the first and second addresses, and all successive addresses are selected between the selected first and second addresses, to thereby accomplish selection of addresses of a successive range.

5. The frame memory device of claim 4, wherein each of the range selectable column address decoder and the range selectable row address decoder is a 8-to-256 range selectable decoder, and wherein the 8-to-256 range selectable decoder comprises:

an exclusive OR gate which judges whether or not values of four upper bits in the two high and low address inputs equal one other, and selects only one group if the values of four upper bits equal one another, but selects two or more groups if the values of four upper bits do not equal one another, to thereby generate an output selection signal with respect to a multiplexer;

a group selection circuit having a first range selectable address decoder for selecting a range between four upper bits of the two high and low addresses, and generating a low enable signal, a middle enable signal, and a high enable signal which select a low group, a middle group and a high group, respectively, if four upper bits of the two high and low address inputs do not equal one another;

a second range selectable decoder for selecting a range value between "1111" and four lower bits of a low address input value in order to select a low address range among 16 addresses in the low group selected by the four lower bits of the low address input;

a third range selectable decoder for selecting a range value between "0000" and four lower bits of a high address input value in order to select a high address range among 16 addresses in the high group selected by the four lower bits of the high address input;

a first multiplexer for selectively outputting any one input among the four lower bits of the low address input and the "0000" to the third range selectable decoder, according to an output of the group selection circuit;

a second multiplexer group having 16 multiplexers, in which "0" is input to one input terminal of each multiplexer and a low enable signal is input to the other terminal thereof, and the output of the group selection circuit is input as an output selection signal;

a third multiplexer group having 16 multiplexers, in which "0" is input to one input of each multiplexer and a middle enable signal is input to the other input thereof, and the output of the group selection circuit is input as an output selection signal;

a fourth multiplexer group having 16 multiplexers, in which the output of the first range selectable decoder is input to one input of each multiplexer and a high enable signal is input to the other input thereof, and the output of the group selection circuit is input as an output selection signal;

a first AND gate group having 16 AND gates in which the output of the second range selectable decoder is connected to one input of each AND gate and each output of the 16 multiplexers in the second multiplexer group is connected to the other input thereof;

a second AND gate group having 16 AND gates in which 16'hffff is applied to one input of each AND gate and each output of the 16 multiplexers in the third multiplexer group is connected to the other input thereof, in order to output "1" to all outputs of the 16 AND gates, so that all addresses between the selected low and high addresses are selected;

a third AND gate group having 16 AND gates in which the output of the third range

selectable decoder is connected to one input of each AND gate and each output of the 16 multiplexers in the fourth multiplexer group is connected to the other input thereof; and

an OR gate for logically summing the outputs of the first through third gate groups.

6. The frame memory device of claim 5, wherein the group selection circuit comprises:

a first range selectable decoder for selecting a range value between four upper bits of each of two high and low address inputs;

a right shift register for shifting the output of the first range selectable decoder by one bit to the right;

a left shift register for shifting the output of the first range selectable decoder by one bit to the left;

a first inverter for inverting the output of the right shift register;

a second inverter for inverting the output of the left shift register;

a low enable signal generator for generating a low enable signal which selects and enables a low group in combination with the output of the right shift register, the output of the first range selectable decoder, and the output of the first inverter;

a middle enable signal generator for generating a middle enable signal which selects and enables a middle group in combination with the output of the right shift register, the output of the first range selectable decoder, and the output of the left shift register; and

a high enable signal generator for generating a high enable signal which selects and enables a high group in combination with the output of the second inverter, the output of the first range selectable decoder, and the output of the left shift register.

7. The frame memory device of claim 5, wherein if the four upper bits of the two high and low address inputs are same one another, the group selection circuit selects only one group, so that all the outputs of the first multiplexer and the second through fourth multiplexers are selected as zero port input to thus have all the outputs of the first and second AND gate groups

selected as "0", and

wherein one bit of the output of the first range selectable decoder and all 16 bits of the output of the third range selectable decoder are logically ANDed in the third AND gate group formed of 16 AND gates, to thereby generate column and row address selection signals.

8. The frame memory device of claim 5, wherein if the four upper bits of the two high and low address inputs are not same one another, the group selection circuit generates a group enable signal for selecting a number of groups, and thus all the outputs of the first multiplexer and the second through fourth multiplexer groups are selected as "1" port input, so that the low address range belonging to the low group selected from the first AND gate group is selected by the output of the second range selectable decoder, the middle address range belonging to the middle group selected from the second AND gate group is selected, the high address range belonging to the high group selected from the third AND gate group is selected by the output of the third range selectable decoder.

9. The frame memory device of claim 5, wherein each of the first through third range selectable decoders is a 4-to-16 range selectable decoder, and wherein the 4-to-16 range selectable address decoder comprises:

a first general purpose decoder for generating a 16-bit decoded output when the four-bit low address is applied thereto;

a second general purpose decoder for generating a 16-bit decoded output when the four-bit high address is applied thereto; and

first through thirtieth XOR gates for processing first through sixteenth outputs of the first general purpose decoder and first through sixteenth outputs of the second decoder, and selecting a range value between the low address and the high address.

10. The frame memory device of claim 8, wherein each of the first through third range

selectable decoders is a 4-to-16 range selectable decoder, and wherein the 4-to-16 range selectable address decoder comprises:

a first general purpose decoder for generating a 16-bit decoded output when the four-bit low address is applied thereto;

a second general purpose decoder for generating a 16-bit decoded output when the four-bit high address is applied thereto; and

first through thirtieth XOR gates for processing first through sixteenth outputs of the first decoder and first through sixteenth outputs of the second decoder, and selecting a range value between the low address and the high address.

11. The frame memory device of claim 1, wherein each of the range selectable column address decoder and the range selectable row address decoder is a 8-to-256 range selectable decoder.

12. The frame memory device of claim 11, wherein each of the range selectable column address decoder and the range selectable row address decoder performs selection of an address of a successive range, respectively, in which the total 256 addresses are divided into 16 groups in the case that the first and second column addresses and the first and second row addresses are 8-bit signals, respectively, a corresponding group by respective four upper bits of the first and second address inputs in units of 16 addresses, a low address range is selected among 16 addresses in the group selected by four lower bits of the low address input among the first and second addresses, a high address range is selected among 16 addresses in the group selected by four lower bits of the high address input among the first and second addresses, and all successive addresses are selected between the selected first and second addresses, to thereby accomplish selection of addresses of a successive range.

13. A frame memory device comprising:

a number of memory cells aligned in a matrix form;

a range selectable column address decoder for receiving high and low column addresses and generating at least one column address selection signal in order to designate at least one column address range with respect to the number of memory cells; and

a general purpose row address decoder for receiving high and low row addresses and generating two row address selection signals in order to designate two row addresses with respect to the number of memory cells,

wherein memory cells located from a low column address to a high column address designated by the range selectable column address decoder, are designated on two row lines designated by the general purpose row address decoder according to the input of the high and low row addresses, to thereby write graphic data of two parallel lines that are parallel with the X-axis.

14. The frame memory device of claim 13, wherein the range selectable column address decoder comprises a 8-to-256 range selectable decoder, and

the general purpose row address decoder comprises:

first and second general purpose 8-to-256 decoders for enabling one output among 256 outputs when 8-bit high and low addresses are input thereto; and

first through 256th OR gates for logically summing the outputs of an identical level from the first and second 8-to-256 decoders.

15. A frame memory device comprising:

a number of memory cells aligned in a matrix form;

a range selectable row address decoder for receiving high and low row addresses and generating at least one row address selection signal in order to designate at least one row address range with respect to the number of memory cells; and

a general purpose column address decoder for receiving high and low column addresses

and generating two column address selection signals in order to designate two column addresses with respect to the number of memory cells,

wherein memory cells located from a low row address to a high row address which are designated by the range selectable address decoder, are designated on two column lines designated by the general purpose column address decoder according to the input of the high and low row addresses, to thereby write graphic data of two parallel lines that are parallel with the Y-axis.

16. A frame memory device comprising:

a number of memory cells aligned in a matrix form;

a first general purpose decoder for receiving high and low column addresses and generating two column address selection signals to designate two column addresses with respect to the number of memory cells; and

a second general purpose decoder for receiving high and low row addresses and generating two row address selection signals to designate two row addresses with respect to the number of memory cells,

wherein graphic data is written by a single write operation all at a time, in four memory cells of a point where two row lines designated by the second general purpose address decoder according to the input of the high and low row addresses and two column lines designated by the first general purpose address decoder according to the input of the high and low column addresses cross-sect each other.

17. The frame memory device of claim 16, wherein each of the first and second general purpose address decoders comprises:

first and second general purpose 8-to-256 decoders for enabling one output among 256 outputs when 8-bit high and low addresses are input thereto; and

first through 256th OR gates for logically summing the outputs of an identical level from

the first and second 8-to-256 decoders.

18. An 8-to-256 range selectable decoder for selecting a successive range value between a high address and a low address when 8-bit high and low addresses are applied thereto, the 8-to-256 range selectable decoder comprises:

an exclusive OR gate which judges whether or not values of four upper bits in the two high and low address inputs equal one other, and selects only one group if the values of four upper bits equal one another, but selects two or more groups if the values of four upper bits do not equal one another, to thereby generate an output selection signal with respect to a multiplexer;

a group selection circuit having a first 4-to-16 range selectable address decoder for selecting a range between four upper bits of the two high and low addresses, and generating a low enable signal, a middle enable signal, and a high enable signal which select a low group, a middle group and a high group, respectively, if four upper bits of the two high and low address inputs do not equal one another;

a second 4-to-16 range selectable decoder for selecting a range value between "1111" and four lower bits of a low address input value in order to select a low address range among 16 addresses in the low group selected by the four lower bits of the low address input;

a third 4-to-16 range selectable decoder for selecting a range value between "0000" and four lower bits of a high address input value in order to select a high address range among 16 addresses in the high group selected by the four lower bits of the high address input;

a first multiplexer for selectively outputting any one input among the four lower bits of the low address input and the "0000" to the input terminal of the third 4-to-16 range selectable decoder, according to an output of the group selection circuit;

a second multiplexer group having 16 multiplexers, in which "0" is input to one input terminal of each multiplexer and a low enable signal is input to the other terminal thereof, and the output of the group selection circuit is input as an output selection signal;

a third multiplexer group having 16 multiplexers, in which "0" is input to one input terminal of each multiplexer and a middle enable signal is input to the other terminal thereof, and the output of the group selection circuit is input as an output selection signal;

a fourth multiplexer group having 16 multiplexers, in which the output of the first 4-to-16 range selectable decoder is input to one input terminal of each multiplexer and a high enable signal is input to the other terminal thereof, and the output of the group selection circuit is input as an output selection signal;

a first AND gate group having 16 AND gates in which the output of the second 4-to-16 range selectable decoder is connected to one terminal of each AND gate and each output of the 16 multiplexers in the second multiplexer group is connected to the other input terminal thereof;

a second AND gate group having 16 AND gates in which 16'hffff is applied to one terminal of each AND gate and each output of the 16 multiplexers in the third multiplexer group is connected to the other input terminal thereof, in order to output "1" to all outputs of the 16 AND gates, so that all addresses between the selected low and high addresses are selected;

a third AND gate group having 16 AND gates in which the output of the third 4-to-16 range selectable decoder is connected to one terminal of each AND gate and each output of the 16 multiplexers in the fourth multiplexer group is connected to the other input terminal thereof; and

an OR gate for logically summing the outputs of the first through third gate groups.